Freeform Search

Database: US Pre-Grant Publication Full-Text Database
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Term: L23 and 11

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Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Friday, October 29, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=OR			
L25	L23 and l1	0	L25
L24	L23 and l16	0	L24
L23	(719/329,332)![CCLS]	286	L23
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L22	l16 and (plur$8 or multiple or two or second or multi$9) near5 thread$3	85	L22
L21	L16 and l9	3	L21
L20	L16 and l8	8	L20
L19	L16 and l7	11	L19
L18	L16 and l6	157	L18
L17	L16 and l5	357	L17
L16	L15 and l1	511	L16
L15	(logic$3 or bit near1 wise or "XOR" or exclusive) near5 (register$1 or read$5 or writ$5)	96725	L15
L14	l2 and l9	1	L14
L13	l2 and l8	2	L13

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L12	l2 and l7	8	L12
L11	l2 and l6	92	L11
DB=PGPB,USPT; PLUR=YES; OP=OR			
L10	l2 and l5	282	L10
L9	(710/61,305)![CCLS]	1540	L9
L8	(718/108)![CCLS]	274	L8
L7	(711/145,152,153)![CCLS]	1409	L7
L6	(712/217,223,225,228,247)![CCLS]	1558	L6
L5	(712/2-300)![CCLS]	10394	L5
L4	(712/2-300)![CCLS]	35	L4
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2 near25 (shar$7 or common)	1	L3
L2	L1 near25 (read$6 or writ$6)	339	L2
L1	(remap$7 or renam$4) near8 register$1 near15 (core$1 or entit$4 or thread$4 or program$6 or application$1 or domain$1 block$1)	878	L1

END OF SEARCH HISTORY

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(remap or map or rename) and register and read and | Search

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Results Key:
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1 **The design space of register renaming techniques**
Sima, D.;
Micro, IEEE , Volume: 20 , Issue: 5 , Sept.-Oct. 2000
Pages:70 - 83

[Abstract] [PDF Full-Text (140 KB)] IEEE JNL

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2 **Reducing register ports for higher speed and lower energy**
Park, I.; Powell, M.D.; Vijaykumar, T.N.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Pages:171 - 182

[Abstract] [PDF Full-Text (277 KB)] IEEE CNF

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3 **Complexity-effective reorder buffer designs for superscalar process**
Kucuk, G.; Ponomarev, D.V.; Ergin, O.; Ghose, K.;
Computers, IEEE Transactions on , Volume: 53 , Issue: 6 , June 2004
Pages:653 - 665

[Abstract] [PDF Full-Text (1376 KB)] IEEE JNL

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4 **Register renaming for x86 superscalar design**
Chang-Chung Liu; R-Ming Shiu; Chung-Ping Chung;
Parallel and Distributed Systems, 1996. Proceedings., 1996 International Conference on , 3-6 June 1996
Pages:336 - 343

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5 **Testing the configurability of dynamic FPGAs**
Park, N.; Ruiwale, S.J.; Lombardi, F.;
Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE Internal Symposium on , 25-27 Oct. 2000
Pages:311 - 319

[Abstract] [PDF Full-Text (464 KB)] **IEEE CNF**

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6 **Assignment of storage values to sequential read-write memories**
Gerez, S.H.; Woutersen, E.G.;
Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996
Pages:302 - 308

[Abstract] [PDF Full-Text (604 KB)] **IEEE CNF**

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7 **Register write specialization register read specialization: a path to complexity-effective wide-issue superscalar processors**
Seznec, A.; Toullec, E.; Rochecouste, O.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Pages:383 - 394

[Abstract] [PDF Full-Text (294 KB)] **IEEE CNF**

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8 **A 14-port 3.8 ns 116-word 64b read-renaming register file**
Asato, C.; Montoye, R.; Gmuender, J.; Wade Simmons, E.; Ike, A.; Zasio, J.;
Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC 1995 IEEE International , 15-17 Feb. 1995
Pages:104 - 105, 345

[Abstract] [PDF Full-Text (780 KB)] **IEEE CNF**

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rename and register and read and write Search

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